AMENDMENTS TO THE CLAIMS

Claim 1 (Original): An IC chip, comprising:

a substrate;

an integrated circuit formed on the substrate and having at least one first electrical conductor and at least one region in which external electromagnetic or radioactive irradiation causes a malfunction;

a second electrical conductor formed in the substrate and in which external electromagnetic or radioactive irradiation generates free charge carriers which give rise to a current flow in and during operation of the integrated circuit; and

a protective structure that detects the rise in the current flow, thereby indicating a malfunction caused by the irradiation.

Claim 2 (Original): The IC chip as claimed in claim 1, further comprising:

a plurality of first electrical conductors provided as data lines and having interconnects,

wherein the second electrical conductor is a doped region formed in the substrate and arranged parallel to a respective interconnect.

Claim 3 (Original): The IC chip as claimed in claim 1, wherein the at least one first electrical conductor is spaced apart from the second electrical conductor.

Claim 4 (Original): The IC chip as claimed in claim 1, wherein the second electrical conductor is laterally offset with respect to the at least one first electrical conductor.

Claim 5 (Original): The IC chip as claimed in claim 1, wherein there are a plurality of first electrical conductors, and the second electrical conductor has strip-type doped regions arranged between the regions of the substrate provided with the first electrical conductors.

Claim 6 (Original): The IC chip as claimed in claim 1, wherein the integrated circuit is part of an EEPROM.

Claim 7 (Original): A smart card comprising the IC chip of claim 1.

Claim 8 (Original): A chip module comprising the IC chip of claim 1.

Claim 9 (Original): An IC chip, comprising:

a memory;

at least one first data line transmitting information data; and

at least one second data line arranged in a vicinity of the at least one first data line and transmitting test data used to determine whether the information data transmitted on the at least one first data line is corrupted;

wherein external electromagnetic or radioactive irradiation that changes the information data transmitted on the first data line also changes the test data transmitted on the at least one second data line.

Claim 10 (Original): The IC chip of claim 9, further comprising a plurality of first data lines, wherein the at least one second data line is arranged between the first data lines.

Claim 11 (Original): The IC chip of claim 9, further comprising a plurality of first data lines and a plurality of second data lines, and wherein the second data lines are interlaced with the first data lines.

Claim 12 (Original): The IC chip as claimed in claim 9, wherein the at least one second data line transmits a check digit, a check number or code number, which results, in an unambiguously determined manner, from the transmitted data.

Claim 13 (Original): The IC chip as claimed in one of claim 9 wherein the memory is an EEPROM.

Claim 14 (Original): A smart card comprising the IC chip of claim 9.

Claim 15 (Original): A chip module comprising the IC chip of claim 9.

Claim 16 (Original): An IC chip, comprising:

a semiconductor material;

one or more metallization planes; and

a dielectric covering the one or more metallization planes and having a relative permittivity that changes to an extent that is relevant in terms of circuitry under an influence of external electromagnetic or radioactive irradiation;

wherein the dielectric is provided at least above or below a particular metallization plane or within a layer formed by the one or more metallization planes.

Claim 17 (Original): The IC chip as claimed in claim 16, further comprising:

two metallization planes having the dielectric provided therebetween; and

an integrated circuit that detects a change in electrical capacitance between the two metallization planes.

Claim 18 (Original): The IC chip as claimed in claim 16, wherein a metallization plane of the one or more metallization planes is patterned in parts that are electrically insulated from one another by the dielectric, and

further comprising an integrated circuit that detects a change in electrical capacitance between the parts.

Claim 19 (Original): A smart card comprising the IC chip of claim 16.

Claim 20 (Original): A chip module comprising the IC chip of claim 16.

Claim 21 (Original): An IC chip, comprising:

electrical conductors;

a connection connecting the electrical conductors and including a material, the electrical resistance of which decreases under an external electromagnetic or radioactive irradiation; and

a circuit that detects the decrease in the electrical resistance of the connection.

Claim 22 (Original): A smart card comprising the IC chip of claim 21.

Claim 23 (Original): A chip module comprising the IC chip of claim 21.